PALLV22V10 Family

Low-Voltage 24-Pin EE CMOS Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Low-voltage operation, 3.3 V JEDEC compatible**
  - V_{CC} = + 3.0 V to 3.6 V
- **Commercial operating temperature range**
- **7.5-ns t_{PD}**
- **Electrically-erasable technology provides reconfigurable logic and full testability**
- **10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs**
- **Varied product term distribution allows up to 16 product terms per output for complex functions**
- **Global asynchronous reset and synchronous preset for initialization**
- **Power-up reset for initialization and register preload for testability**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **24-pin SKINNYDIP and 28-pin PLCC packages save space**

GENERAL DESCRIPTION

The PALLV22V10 is an advanced PAL device built with low-voltage, high-speed, electrically-erasable CMOS technology.

The PALLV22V10 device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PALLV22V10 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar.

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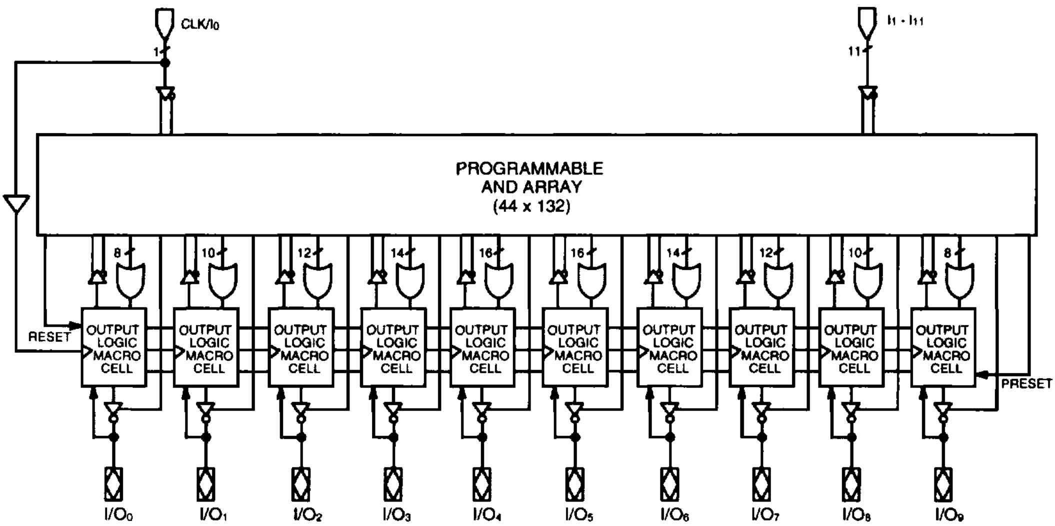
BLOCK DIAGRAM



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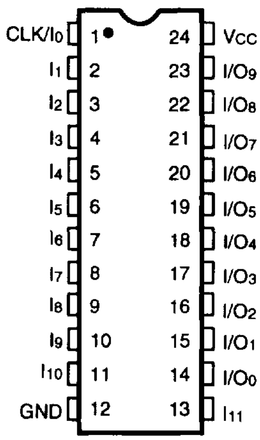
CONNECTION DIAGRAMS

Top View

SKINNYDIP



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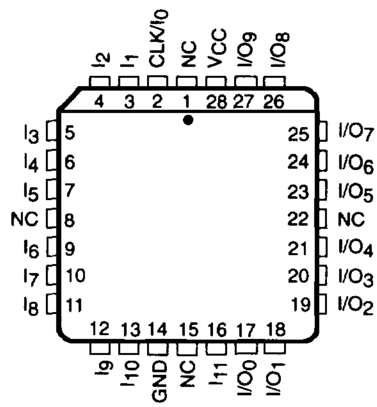
PLCC



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Note:
Pin 1 is marked for orientation.

PIN DESCRIPTION

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of these elements:

PAL LV 22 V 10 7 J C

FAMILY TYPE
PAL = Programmable Array Logic

TECHNOLOGY
LV = Low-Voltage

NUMBER OF ARRAY INPUTS

OUTPUT TYPE
V = Versatile

NUMBER OF OUTPUTS

OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

PACKAGE TYPE
P = 24-Pin 300 mil Plastic SKINNYDIP (PD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)

SPEED
-7 = 7.5 ns t_{PD}
-10 = 10 ns t_{PD}
-15 = 15 ns t_{PD}

Valid Combinations	
PALLV22V10-7	JC
PALLV22V10-10	PC, JC
PALLV22V10-15	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PALLV22V10 is the low-voltage version of the PALCE22V10. It has all the architectural features of the PALCE22V10.

The PALLV22V10 allows the systems engineer to implement a design on-chip by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALLV22V10 has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active-high or active-low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 - S_1. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

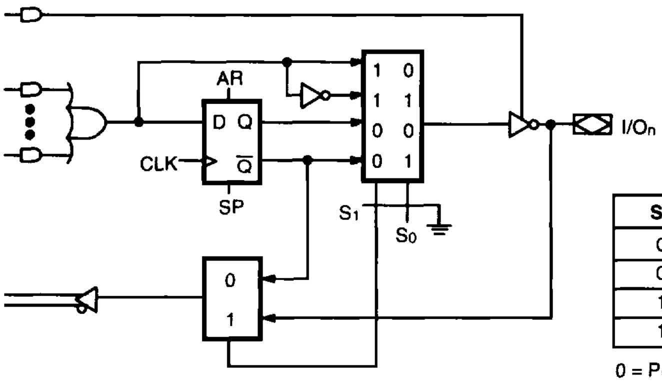
The PALLV22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Registered Output Configuration

Each macrocell of the PALLV22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

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Figure 1. Output Logic Macrocell

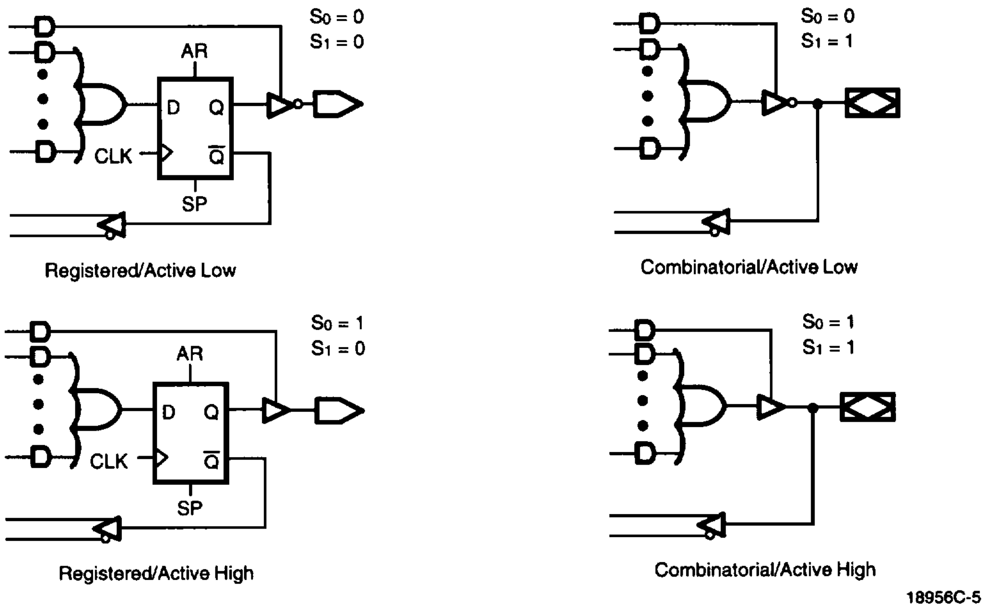


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALLV22V10 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Benefits of Lower Operating Voltage

The PALLV22V10 has an operating voltage range of 3.0 V to 3.6 V. Low voltage allows for lower operating power consumption, longer battery life, and/or smaller batteries for notebook applications.

Because power is proportional to the square of the voltage, reduction of the supply voltage from 5.0 V to 3.3 V significantly reduces power consumption. This directly translates to longer battery life for portable applications. Lower power consumption can also be used to reduce the size and weight of the battery. Thus, 3.3 V designs facilitate a reduction in the form factor.

A lower operating voltage results in a reduction of I/O voltage swings. This reduces noise generation and provides a less hostile environment for board design. Lower operating voltage also reduces electromagnetic radiation noise and makes obtaining FCC approval easier.

3.3-V (CMOS) and 5-V (CMOS and TTL) Compatible Inputs and I/O

Input voltages can be at TTL levels. Additionally, the PALLV22V10 can be driven with true 5-V CMOS levels due to special input and I/O buffer circuitry.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PALLV22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum. Details on power-up reset can be found on page 14.

Register Preload

The registers on the PALLV22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALLV22V10 design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALLV22V10 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required. Approved programmers are listed on page 17.

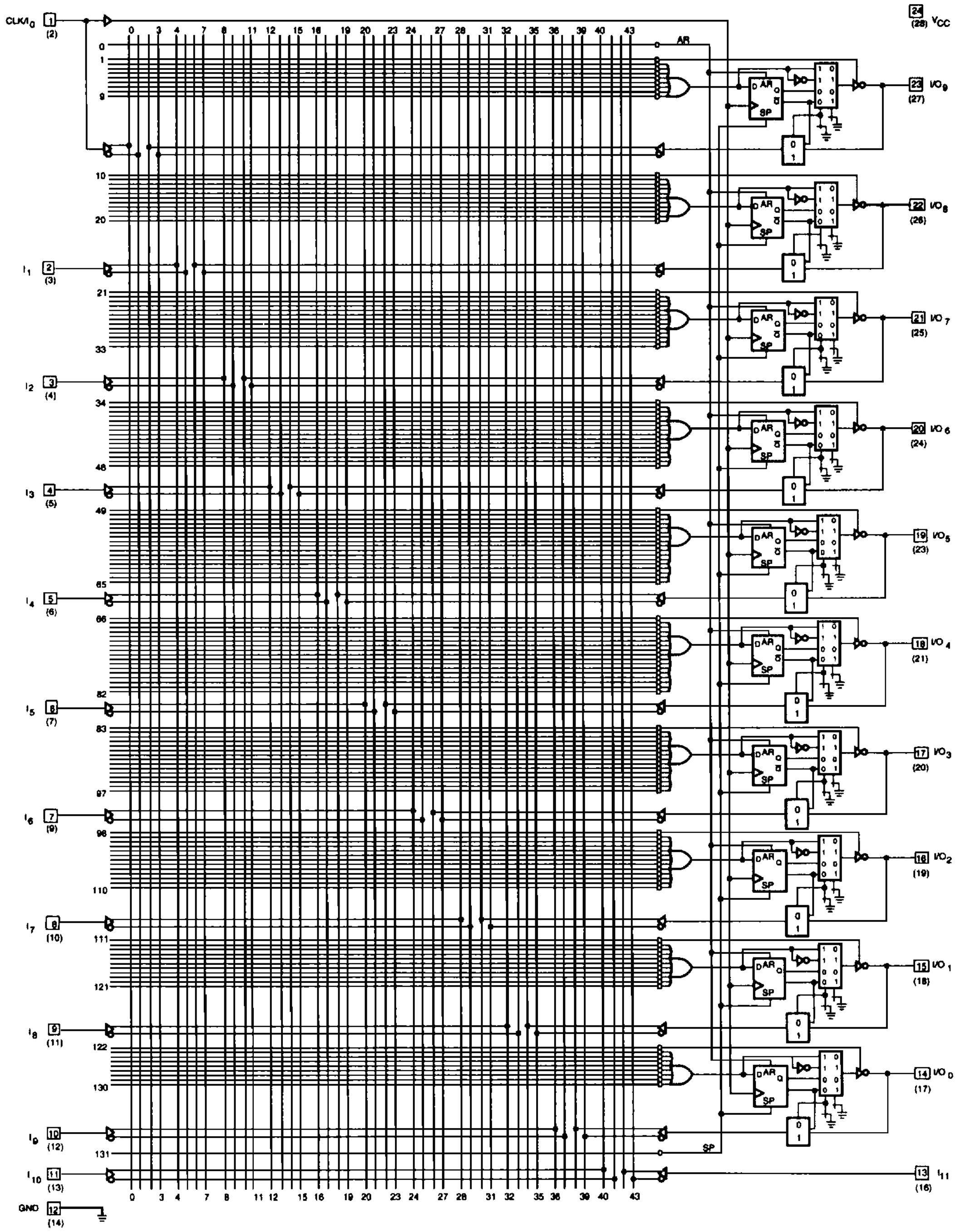
Quality and Testability

The PALLV22V10 offers a very high level of built-in quality. The erasability of the CMOS PALLV22V10 allows direct testing of the device array to guarantee 100% programming and functional yields.

Technology

The high-speed PALLV22V10 is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be 3.3 V and 5 V device compatible. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
SKINNYDIP (PLCC) Pinouts



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied .... –55°C to +125°C

Supply Voltage with Respect to Ground .... –0.5 V to +7.0 V

DC Input Voltage .... –0.5 V to +5.25 V

DC Output or I/O Pin Voltage .... –0.5 V to +5.25 V

Static Discharge Voltage .... 2001 V

Latchup Current (0°C to +75°C) .... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Operating Case Temperature (T_A) .... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground .... +3.0 V to +3.6 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -2$ mA	2.4		V
		V_{CC} = Min	$I_{OH} = -100$ µA	V_{CC} –0.2		V
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 16$ mA		0.5	V
			$I_{OL} = 100$ µA		0.2	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0	5.25	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = V_{CC}$, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = V_{CC}$, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–5	–75	mA
I_{CC} (Static)	Supply Current	Outputs f = 0 MHz, Open (I_{OUT} = 0 mA)	-10/15		–60	mA
I_{CC} (Static)			-7		75	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 3.3 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

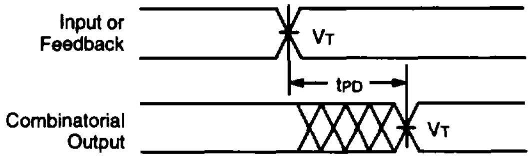
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-7		-10		-15		Unit
				Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				7.5		10		15	ns
t_{S1}	Setup Time from Input, Feedback or SP to Clock			4.5		5.5		10		ns
t_{S2}	Setup Time from SP to Clock			5.5		7		10		ns
t_H	Hold Time			0		0		0		ns
t_{CO}	Clock to Output				5.5		6.5		10	ns
t_{AR}	Asynchronous Reset to Registered Output				11		13		20	ns
t_{ARW}	Asynchronous Reset Width			6		8		10		ns
t_{ARR}	Asynchronous Reset Recovery Time			6		8		10		ns
t_{SPR}	Synchronous Preset Recovery Time			6		8		10		ns
t_{WL}	Clock Width	LOW		3.5		4		6		ns
t_{WH}		HIGH		3.5		4		6		ns
f_{MAX}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_S + t_{CO})$	100		83.3		50		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$	133		110		58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	143		125		83.3		MHz
t_{EA}	Input to Output Enable Using Product Term Control				9		11		15	ns
t_{ER}	Input to Output Disable Using Product Term Control				10		11		15	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:* *$t_{CF} = 1/f_{MAX}$ (internal feedback) $- t_S$.*

SWITCHING WAVEFORMS



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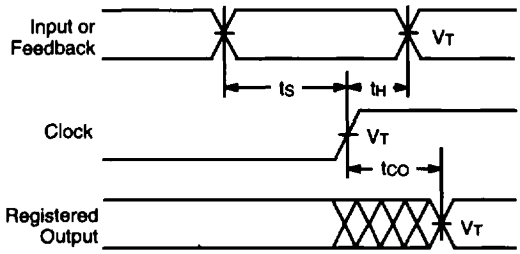
Combinatorial Output



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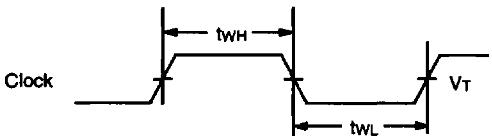
Registered Output



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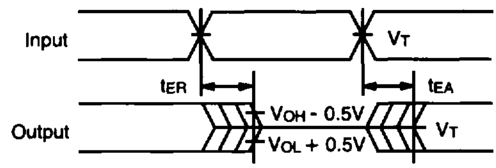
Clock Width



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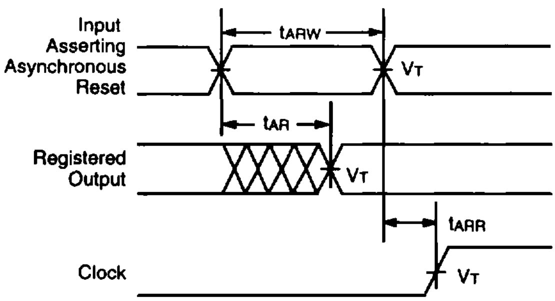
Input to Output Disable/Enable



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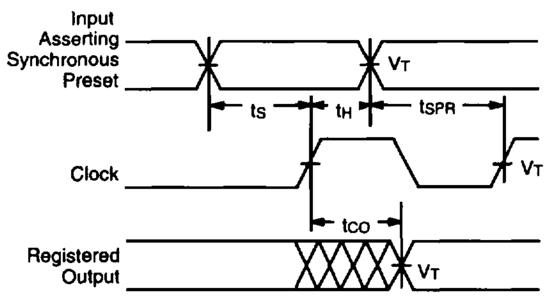
Asynchronous Reset



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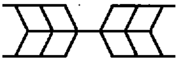
Synchronous Preset

Notes:

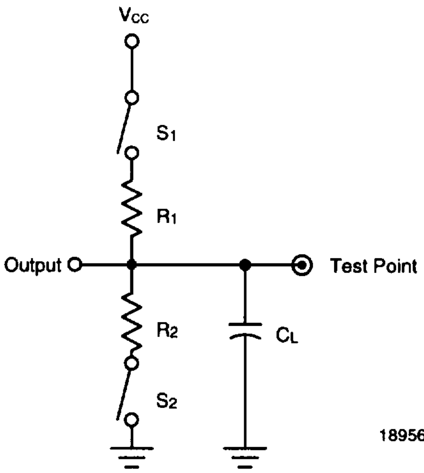
1. *V_T = 1.5 V for inputs signals and $V_{CC}/2$ for outputs signals.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 5 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



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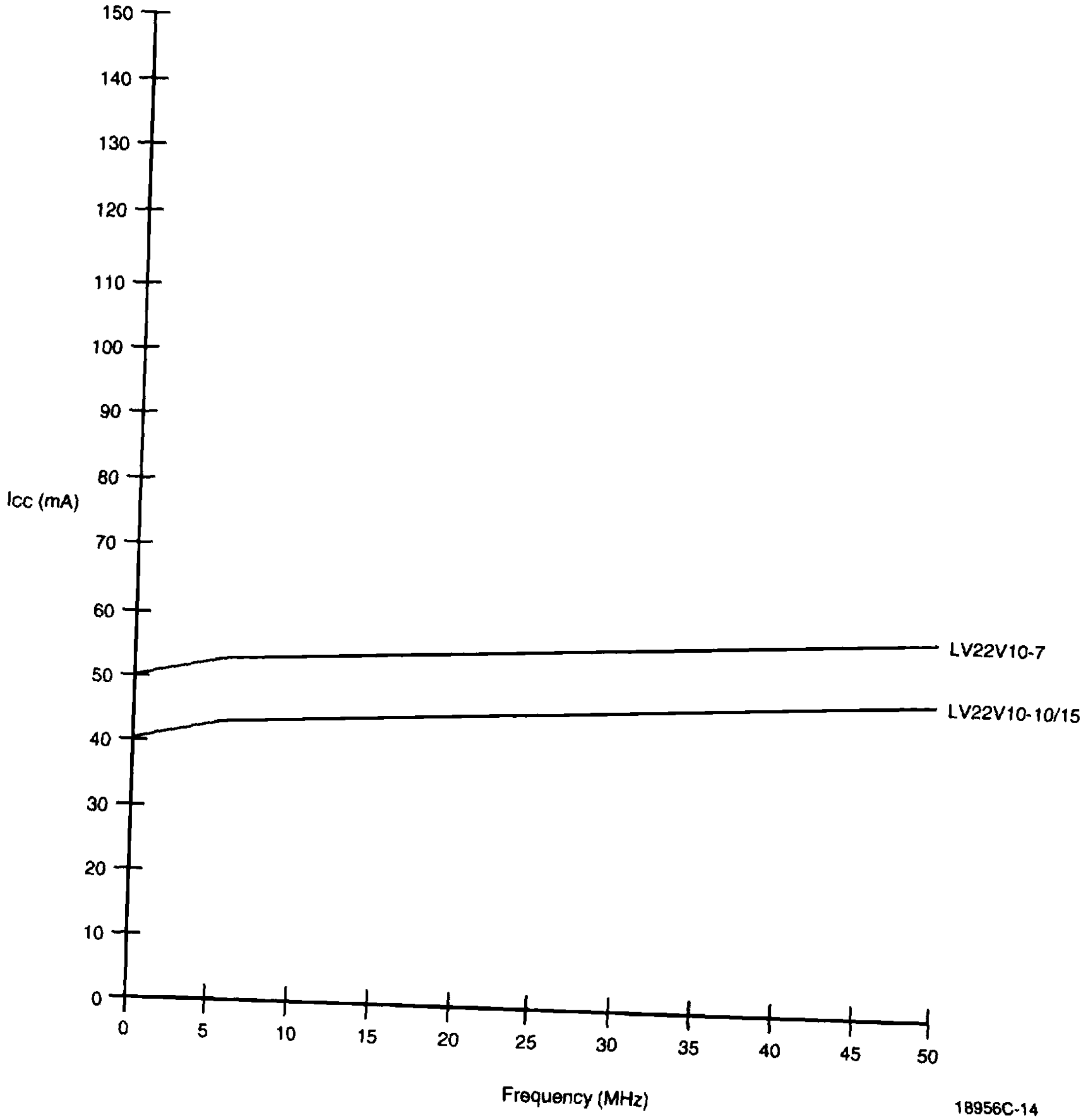
Specification	S_1	S_2	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	Closed	30 pF	1.6K Ω	1.6K Ω	$V_{CC}/2$
t_{EA}	Z → H: Open Z → L: Closed	Z → H: Closed Z → L: Open				$V_{CC}/2$
t_{ER}	H → Z: Open L → Z: Closed	H → Z: Closed L → Z: Open	5 pF			H → Z: $V_{OH} - 0.5$ V L → Z: $V_{OL} + 0.5$ V

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 3.3 V, T_A = 25°C



Icc vs. Frequency

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_{CC}. From this midpoint, a designer may scale the I_{CC} graphs up or down to estimate the I_{CC} requirements for a particular design.

f_{MAX} Parameters

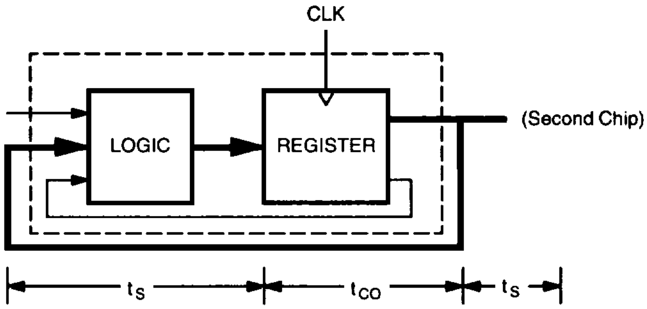
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

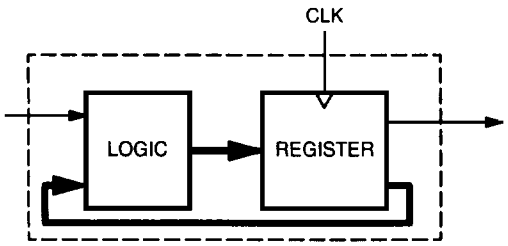
The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design, therefore, this parameter is sometimes called "f_{CNT}."

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

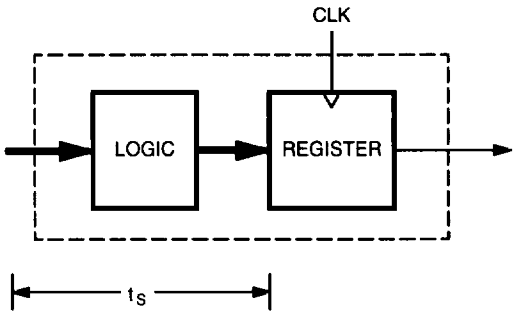
f_{MAX} external and f_{MAX} no feedback are calculated parameters. f_{MAX} external is calculated from t_S and t_{CO}, and f_{MAX} no feedback is calculated from t_{WL} and t_{WH}. f_{MAX} internal is measured.



f_{MAX} External; $1/(t_S + t_{CO})$



f_{MAX} Internal (f_{CNT})



f_{MAX} No Feedback; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$

18956C-15

ENDURANCE CHARACTERISTICS

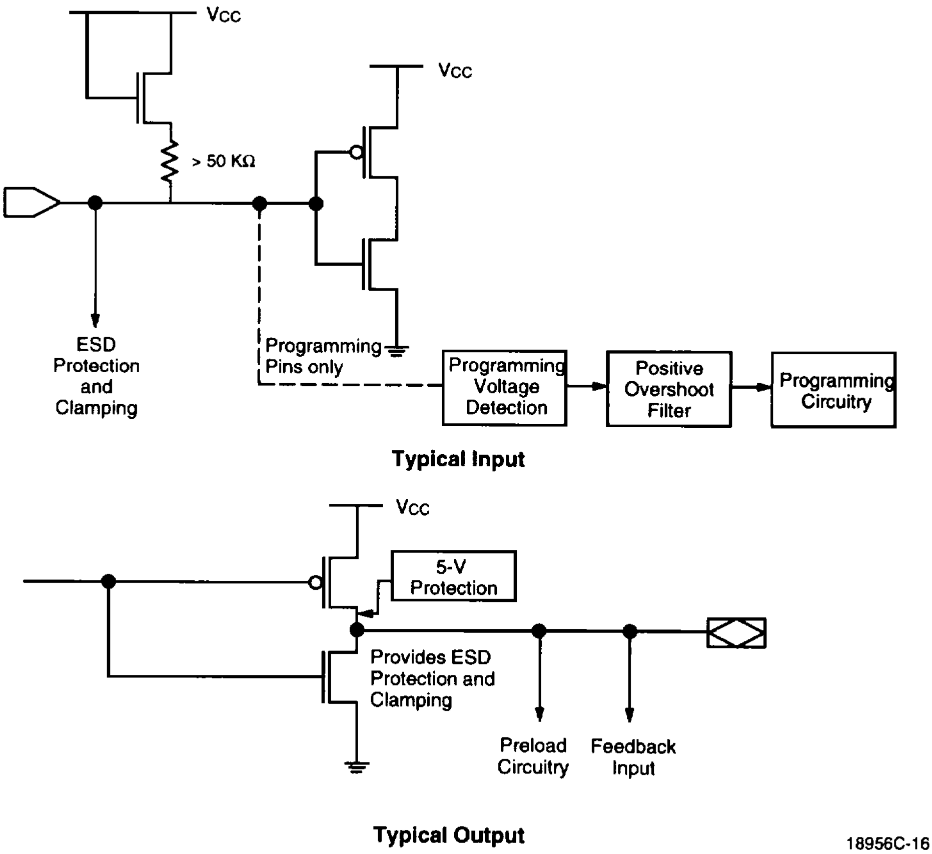
The PALLV22V10 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Symbol	Parameter	Test Conditions	Min	Unit
t_{DR}	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

ROBUSTNESS FEATURES

The PALLV22V10 has some unique features that make it extremely robust, especially when operating in high speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS

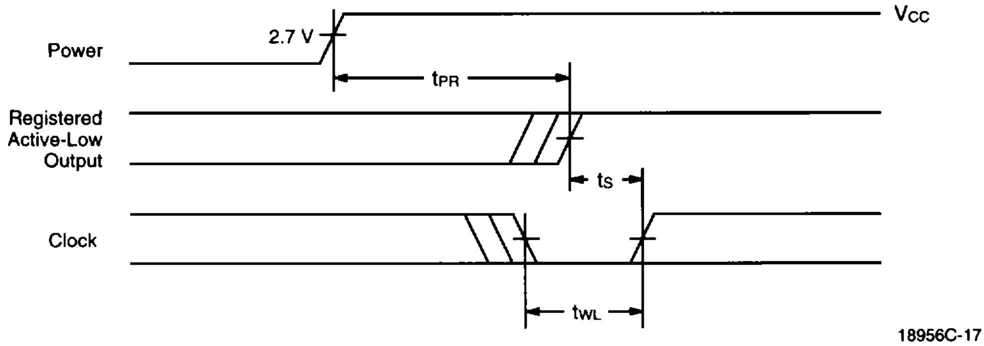


POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The V_{CC} rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-Up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS

PALLV22V10-10

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ SKINNYDIP	Typ PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		26	20	°C/W
θ_{ja}	Thermal impedance, junction to ambient		86	69	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	72	57	°C/W
		400 lfpm air	65	52	°C/W
		600 lfpm air	60	47	°C/W
		800 lfpm air	55	45	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.